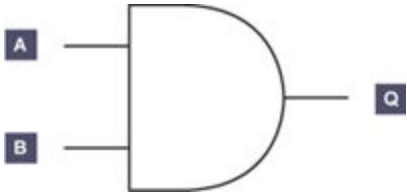


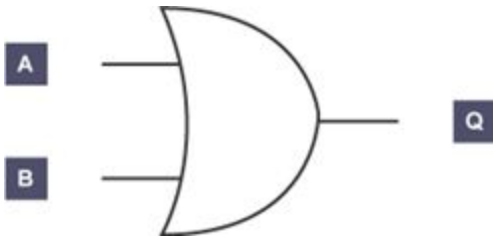
# Logic Gates

## AND gate



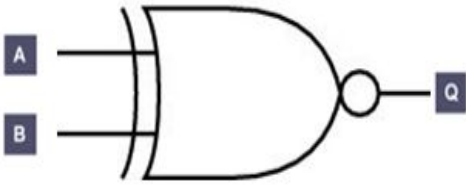
A	B	Q/Output
0	0	
1	0	
0	1	
1	1	

## OR gate



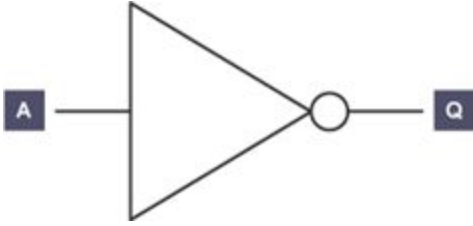
A	B	Q/Output
0	0	
1	0	
0	1	
1	1	

## XOR gate



A	B	Q/Output
0	0	
1	0	
0	1	
1	1	

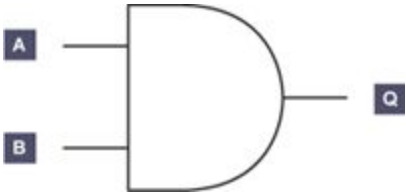
# NOT gate



A	Q/Output
0	
1	

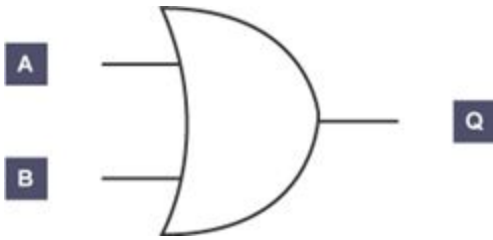
## Logic Gates 2

### AND gate



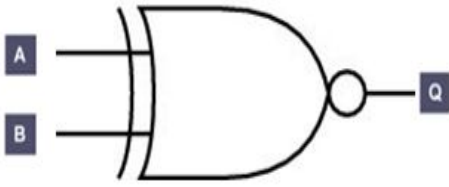
A	B	Q/Output
		0
		0
		0
		1

## OR gate



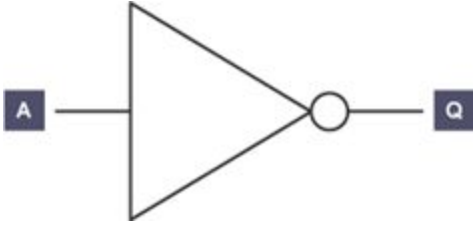
A	B	Q/Output
		0
		1
		1
		1

# XOR gate



A	B	Q/Output
		0
		1
		1
		0

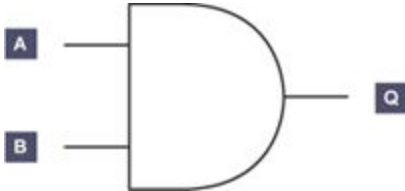
NOT gate



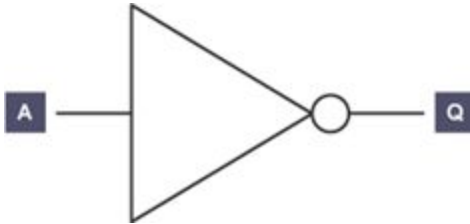
A	Q/Output
	1
	0



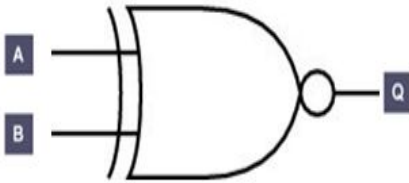
# Logic gates 3



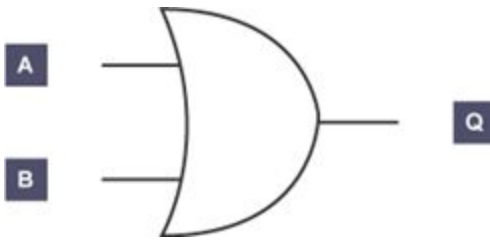
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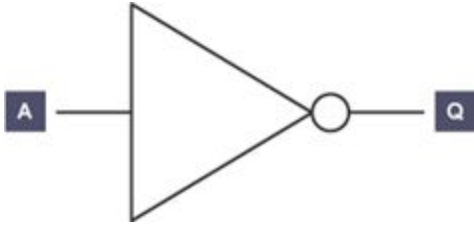


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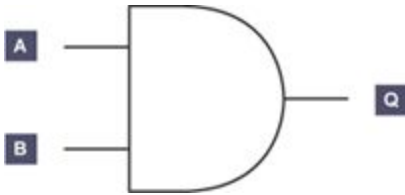


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# Logic Gates 4

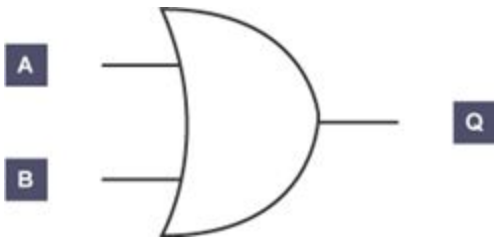


AND gate



NOT gate

OR gate



XOR gate

## Logic Gates 4

Draw an AND gate:

Draw an XOR gate:

Draw a NOT gate:

Draw an OR gate:

<https://scratch.mit.edu/projects/12583438/>

<http://www.neuroproductions.be/logic-lab/>

<https://www.wisc-online.com/learn/technical/electronics-digital/dig2202/the-logic-gates>